in a groove, and both claims recite controlling the formation of the copper film to avoid forming a native oxide. For this reason alone, the applicants respectfully submit that claims 29 and 40 are patentably distinguishable over the prior art of record and therefore in condition for allowance.

The applicants would like to provide the following brief comments regarding claim 29. Claim 29 recites removing a part of the portion of the second insulating film which is exposed to the groove, and a part of the first insulating film under the portion of the second insulating film using the same etching mask. Such as process does not require etching selectivity between the first and second films and can simplify the etching process. Also, the portion of the second insulating film is removed after the groove is formed in the third insulating film. Accordingly, alignment of the second insulating film is easy to perform.

Such a method is not disclosed or suggested in the prior art. In Chow et al., insulating layers 5, 6 and 8 are successively formed on layer 3. Layer 6, an etch stop material such as aluminum oxide is deposited and patterned to provide windows 7 at each location where a stud via connection is to be formed. As shown in Fig. 4, layer 8 is etched and the etching terminates on etch stop layer 6 but continues to etch layer 5 where holes 7 exist. Regions 4 are exposed and, subsequently, metal 9 is deposited to form stud connections and conductors.

As recognized in the Office Action, there is no disclosure or suggestion in Chow et al. of etching first and second films using the same mask as recited in claim 29.

The Office Action looks to Mu et al. to cure this deficiency in Chow et al. The Office Action refers to column 6, lines 8-15 where films 22 and 23 are etched in a single etching step to form a contact hole 30 over region 21 as shown in Fig. 3. Examiner Maldonado, during the interview, also pointed to column 3, lines 18-31 of Mu et al. describing the benefits of an etch stop layer in forming interconnect channels. This is shown, for example,

in Fig. 5 where interconnect channel 51 (right-hand side) stops on material 23. However, this feature is already known from Chow et al., as illustrated in Fig. 4 where the right-hand hole in layer 8 is etched and stops on layer 6, due to layer 6 being an etch stop layer. From this perspective, Mu et al. does not make suggestion for making any modification to Chow et al.

While claim 29 recites removing a portion of the second insulating film which is exposed to the groove and a part of the first insulating film under the portion of the second insulating. The groove is formed in a region of the third insulating film. There is no suggestion of such a process if Mu et al., since the contact opening 30 is formed through films 22 and 23, without reference to any groove in a third insulating film formed over the second insulating film. Looking again at Fig. 5, film 50 is formed and openings 51 are etched, but there is no removing of any portion layers 22 and 23. Channel 30 is filled with the metal 41 and thus there is no etching of the first and second insulating films exposed to a groove formed in a third insulating film. Accordingly, there is clearly no suggestion in Mu et al. of the process recited in claim 29.

As there is no suggestion of the process of claim 29 in either Chow et al. or Mu et al., clearly there can be no suggestion in the combination of the two references, and claim 29 is clearly allowable over any combination of Chow et al. and Mu et al.

During the interview it was explained that the combining of the references would lead to a process where one would begin with Chow et al., form layers 5 and 6, skip the formation of window 7 and form layer 8. Layer 8 would be etched and then a mask would be formed to etch layers 5 and 6 together. However, neither Chow et al. nor Mu et al. disclose or suggest that such a modification should occur. Mu et al. etches layers 22 and 23 without reference to any groove in a third insulating film and Chow et al. specifically rely upon the window 7 in order to form the stud contacts. In Chow et al. the stud contact and the interconnect are formed at the same time, where in Mu et al. the metal 41 is formed prior to forming the

channels 51. Simply two different approaches, neither of which suggests the method of claim 29, are disclosed. Accordingly, there is no suggestion either reference to produce the above described method where the formation of the window 7 would be omitted followed by etching of the films 5 and 6 from a window formed in layer 8.

The Roth et al. patent is relied upon for teaching a passivation layer formed of carbon. Even if such teachings could be combined with that of Chow et al. or Mu et al., one would still not be able to obtain the present invention as recited in claim 29 since there is no suggestion of the etching the first and second insulating films using the same mask as recited in claim 29.

Turning to claim 40, a groove is formed in a third insulating film having a bottom comprising a second insulating film. The forming of groove comprises etching through the second insulating film as to exposed the first insulating film while leaving a remaining second portion of the second insulating film and removing a third portion of the first insulating film to expose the substrate while leaving a remaining portion of the fourth insulating film. There is no suggestion in Chow et al. of forming a groove in a third insulating film with a bottom comprising a second insulating film and the etching through the first and second insulating films. In Chow et al., the window 7 is specifically used in etching through films 5 and 8 at the locations corresponding to window 7, and film 6 is used to prevent the etching of film 5 where no window 7 is formed.

Cochran et al. discloses in Figure 6 a process where films 25 and 27 are etched. There is no groove formed comprising a second film at the bottom. Clearly, there is no suggestion of claim 40 in either of Chow et al. or Cochran et al. and thus claim 40 is clearly patentably distinguishable over a combination of these references.

The present amendment is submitted under provisions of 37 C.F.R. 1.116 governing the entry of amendments after final rejection. As stated in the MPEP §714.12, amendments

placing an application in condition for allowance may be entered. As the amendments to the present invention are clearly believed to distinguish over the prior art, as indicated by Examiner Maldonado during the interview, it is respectfully submitted the entry of the present amendment is proper, and entry thereof is respectfully requested.

It is respectfully submitted that the present application is in condition for allowance and a favorable decision to that effect is respectfully requested.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.

Gregory J. Maier
Attorney of Record
Registration No. 25,599
Carl E. Schlier
Registration No. 34,426

22850
(703) 413-3000
Fax #: (703)413-2220
GJM/CES:maj
I:\atty\CES\00397684.af.wpd

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IN THE CLAIMS

Please amend the claims as follows:

29. (Thrice Amended) A process of fabricating a semiconductor device comprising the steps of:

forming a first insulating film on a semiconductor substrate;

forming a second insulating film on said first insulating film, said second insulating film being made of a material different from that of the first insulating film and having a thickness smaller than that of the first insulating film;

forming a third insulating film on said second insulating film, said third insulating film being made of a material different from that of the second insulating film and having a thickness larger than that of the second insulating film;

forming a groove in a region of said third insulating film, in which a wiring is to be formed, said groove having a bottom to which said second insulating film is exposed;

removing a part of that portion of the second insulating film which is exposed to the groove, and a part of the first insulating film under the portion of the second insulating film, using the same etching mask, and thus forming a contact hole reaching to the semiconductor substrate; and

burying the groove and the contact hole with [a metal] copper to form a [metal] copper wiring in said groove and a [metal] copper contact in said contact hole, and controlling said burying with said copper to avoid formation of a native oxide.

40. (Amended) A process of fabricating a semiconductor device comprising the steps of:

forming a first insulating film on a semiconductor substrate;

forming a second insulating film on said first insulating film, said second insulating film being made of a material different from that of the first insulating film and having a thickness smaller than that of the first insulating film;

forming a third insulating film on said second insulating film, said third insulating film being made of a material different from that of the second insulating film and having a thickness larger than that of the second insulating film;

forming a groove in said third insulating film having a bottom comprising said second insulating film; and

forming copper [a wiring material] in said groove, wherein forming said copper is controlled to avoid formation of a native oxide;

wherein said step of forming said groove comprises;

etching through said second insulation film to expose said first insulation film while leaving a remaining second portion of said second insulation film;

removing a third portion of said first insulation film to expose said substrate while leaving a remaining fourth portion of said first insulation film.